

Uncompromised Throughput at Low Power

Linley Tech Processor Conference
October 5-6, 2011

Per Lembre
Director of Product Marketing

processing
Don't Let Power Ruin Your Power

Content

- The Power Challenge
- Cooling Line Cards
- Scaling NPUs and Staying in Power
- Why Architecture Matters
- Conclusions
- About Xelerated

The Power Challenge

- Information and communication technologies (ICT) accounts for 2-2,5% of world's carbon footprint
- New Facebook site equals to 16,000 households energy consumption
- Bell Labs indicates ICT can be 10,000 times more efficient
- Video to dramatically increase processing and power needs
- Increased push for regulations across Enterprises IT, Service Providers and System and Component Vendors

Green IT: The New Industry Shock Wave Gartner
7 December 2007

Bell Labs to cut the power consumption of the Internet
Steve Bueh
Monday 11 January 2010 18:37

Bell Labs is aiming to cut

Mobile networks to be reworked for energy efficiency, organization demands
Christoph Hammerschmidt
10/23/2009 8:49 AM EDT



Power equals to cost and is a hard limiting factor when designing Carrier Ethernet systems

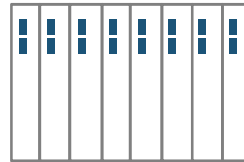
Initiatives to Reduce Power in ICT

Initiative	Objective	Organizations
The Green Grid	Uniting force for global industry efforts, creation of common metrics and tools.	175 members, including chip vendors, service providers and end-users
Digital Agenda for Europe	Ambitious sustainable growth initiative for Europe 2020 where ICT plays critical role	European Commission driving e.g. code of conduct for ICT
Green Touch	Create sustainable Internet through innovation and collaboration	Bell Labs initiative, industry, academia and government
IEEE 802.3AZ	Low-power link state when idle	IEEE members
Global e-Sustainability Initiative (GeSI)	Measurement of ICT impact on climate change	Working together with e.g. ITU
Intellect's Energy Programme	Drive best practice and identify new technologies to reduce carbon footprint	UK tech industry

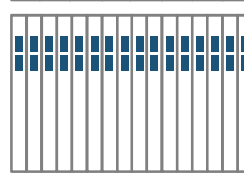
Examples of initiatives to reduce power consumption in the ICT sector

Cooling Line Cards in Central Offices

Power budget mainly limited by air flow engineering in CO and POPs



First generation line cards = 8x 100G



Second generation line cards = 16x 100G in same rack space

- System vendors want to double density and limit power budget per slot
- Traffic interfaces generally not limiting factor
- Many designs at the edge of going one or two slots for new generation line cards

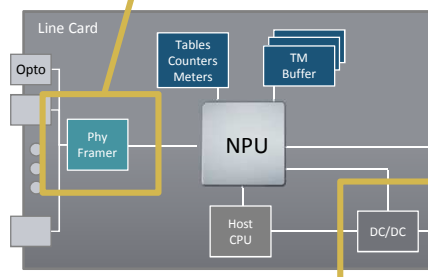
Slide 5

Linley Tech Processor Conference, October 5-6, 2011



The Hotspot Challenge

If individual component is relatively hot, extra cooling techniques may be applied to even dissipation across the board



- Failing to remain within budget will cause PCB re-design
- This opens up for NPU usage in designs where FPGAs or multicores initially selected

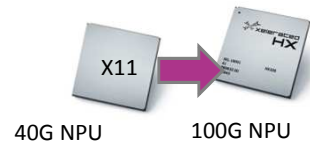
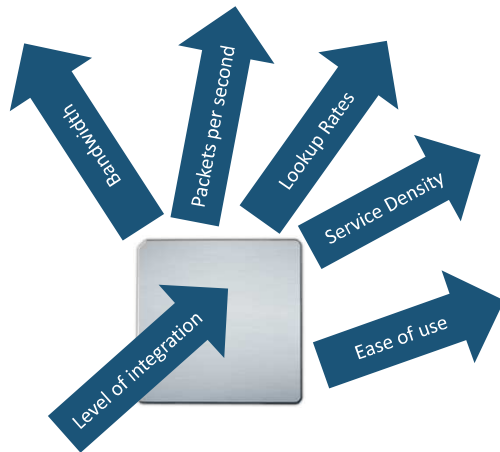
If more power is required, power supply and total PCB layout is affected

Slide 6

Linley Tech Processor Conference, October 5-6, 2011



The Multi-Dimensional Scaling Challenge



Subsystem	Performance
Traffic Interfaces	x2.5
Processing pipeline	x4.2
Advanced Traffic Manager	New!
Embedded switch	New!

In addition to Moore's law of doubling processing power every other year, industry expects less-than proportional increase in energy.

Slide 7

Linley Tech Processor Conference, October 5-6, 2011



Utilize Next-Generation Technology

- Moving from 65nm to 40nm to 28nm gives you more die area to increase integration factor
- NPUs first move was to embed PHY and MACs
- Moving forward more TCAM/SRAM/eDRAM on die makes table lookups more efficient
 - Limits needs to go off-chip for certain applications

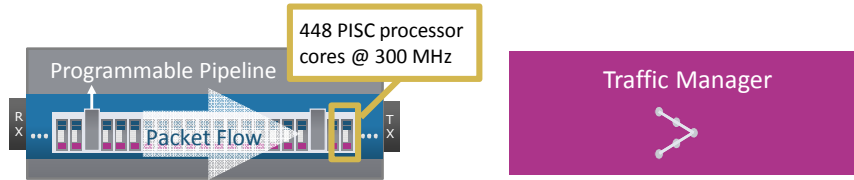
Note! Power leakage increases as geometry decreases

Slide 8

Linley Tech Processor Conference, October 5-6, 2011



Designing for Low Power Starts with Architecture



Dataflow Architecture

- Low clock frequency
=> low power
- Instructions and packet context data always locally available as packet is clocked through the pipeline
- Wirespeed guarantee is priceless
- 100G here today, designed to scale to 200G and 400G

Integrated Traffic Manager

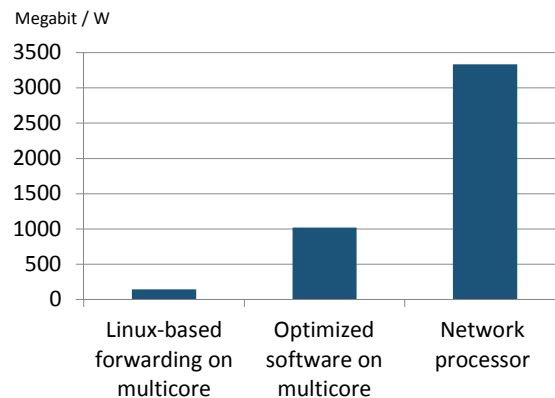
- Integration of TM reduces need for external device at only 5W premium
- Managed pointers in internal memory
- Deep buffering solely in off-chip DDR3 DRAM
- 100G here today, designed to scale to 200G and 400G

Slide 9 Linley Tech Processor Conference, October 5-6, 2011



Throughput per Watt: Architecture Matters

Hardware selection is based on combination of throughput, programmability and power.



Source: <http://www.eejournal.com/archives/articles/20110303-6wind/>, and Xelerated

Slide 10 Linley Tech Processor Conference, October 5-6, 2011



Conclusion

- Power budgets are pushing line card electronics to become more power efficient
- Industry is expecting more than linear reduction of energy as we adopt new technologies
- Architecture and software efficiency can improve power consumption by orders of magnitudes

About Xelerated

Leader in **Carrier Ethernet** Network Processing

- Programmable Chips for Growing Carrier Ethernet Market
 - Network Processors & Programmable Ethernet Switches
 - Data plane software
- Technology Leadership
 - Patented Dataflow Architecture
- Customer Attraction
 - 8 out of 10 of top Carrier Ethernet system vendors
 - Mass-scale network roll-outs in China, Japan, and the US



Outstanding Financial Performance 2009



Winner of Red Herring Europe 100 Award 2010

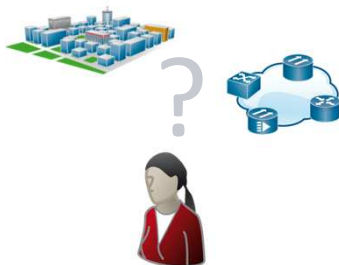
Slide 13 Linley Tech Processor Conference, October 5-6, 2011



Value Through **Technology Leadership**

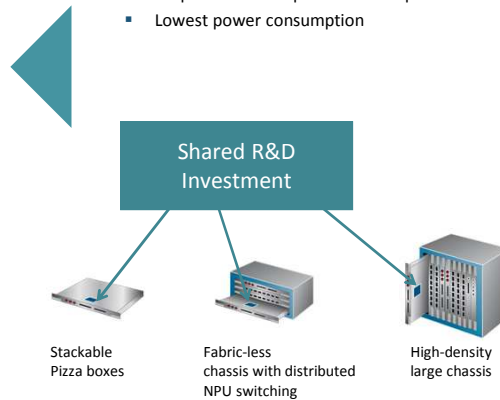
Addressing Key Service Provider Issues...

- Extended product life times
- Headroom for new services
- Deterministic network behavior
- Reduced OPEX



.... By Bringing Value to System Vendors

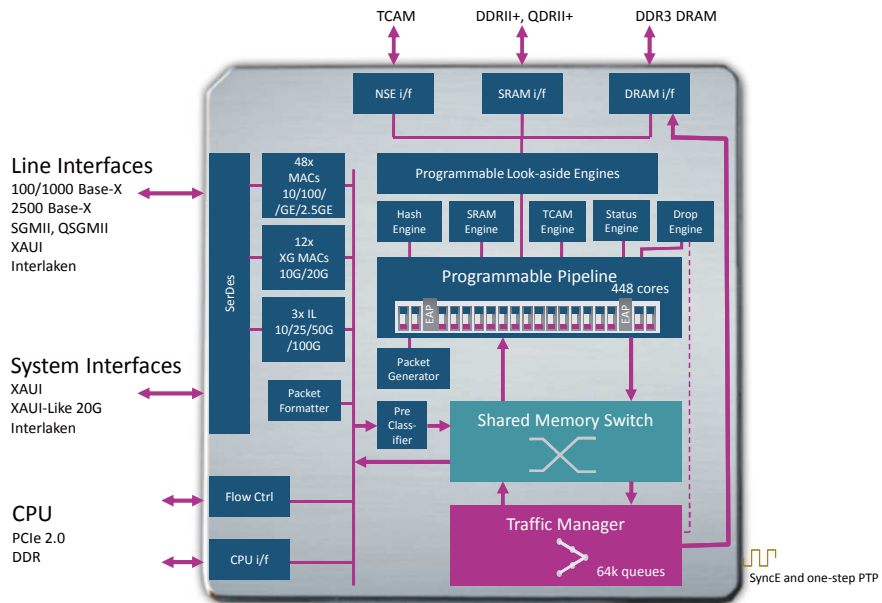
- Programmability for high feature velocity
- Highest service densities
- No performance optimization required
- Lowest power consumption



Slide 14 Linley Tech Processor Conference, October 5-6, 2011



HX 100G Wire-speed NPU with integrated TM

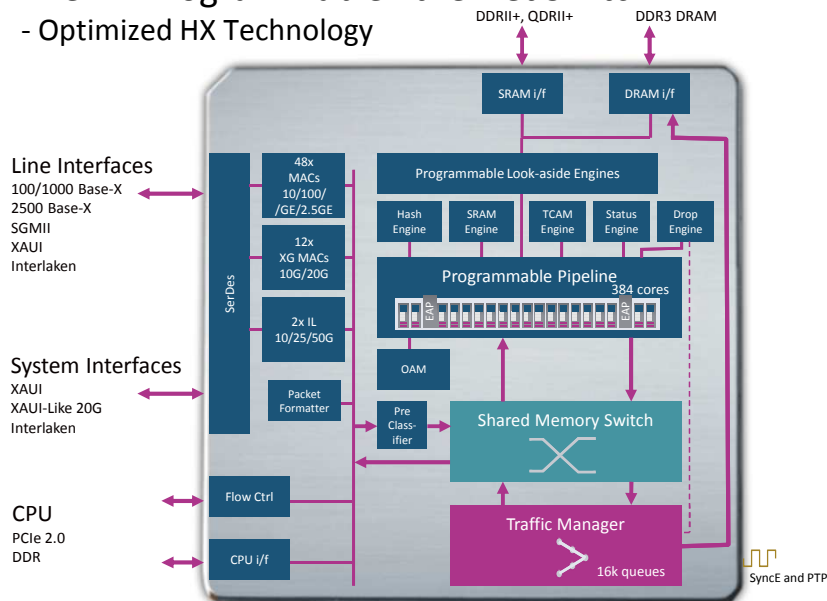


Slide 15 Linley Tech Processor Conference, October 5-6, 2011



The AX Programmable Ethernet Switch

- Optimized HX Technology



Slide 16 Linley Tech Processor Conference, October 5-6, 2011





Wirespeed by Design™

Per Lembre

Director of Product Marketing
per.lembre@xelerated.com

